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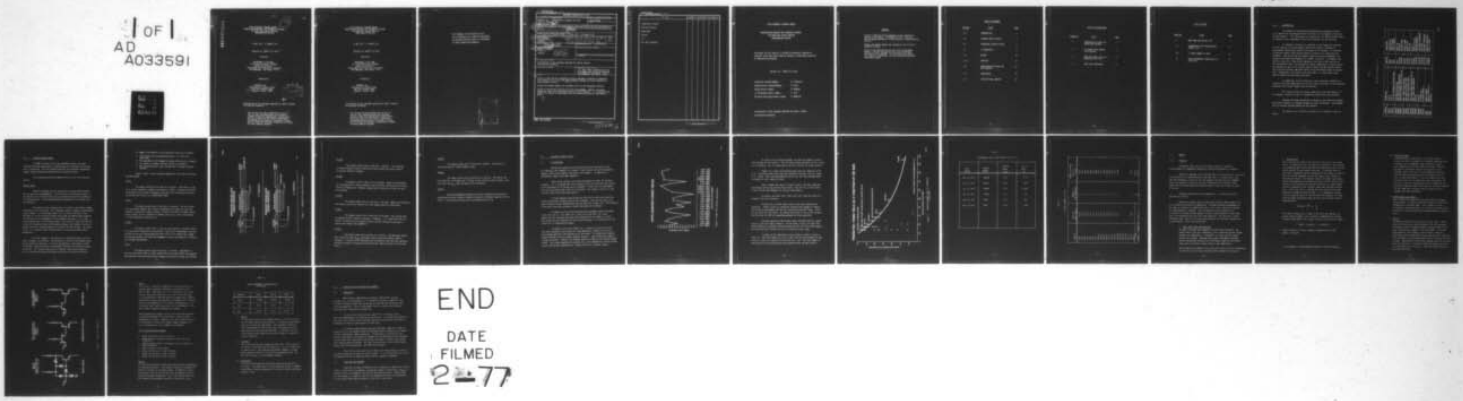

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FIFTH QUARTERLY PROGRESS REPORT MANUFACTURING METHODS AND TECHNOLOGY PROGRAM FOR BEAM LEAD SEALED JUNCTION SEMICONDUCTOR DEVICES

21 MAY 1976 - 21 AUGUST 1976

Contract No. DAAB07-75-C-0033

Placed By

DEPARTMENT OF THE ARMY
U.S. Army Electronics Command
Production Division
Procurement and Production Directorate
Fort Monmouth, New Jersey 07703

Prepared By

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This project has been accomplished as part of the U.S. Army (Manufacturing and Technology) (Advance Production Engineering) Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to insure the efficient production of current or future defense programs.

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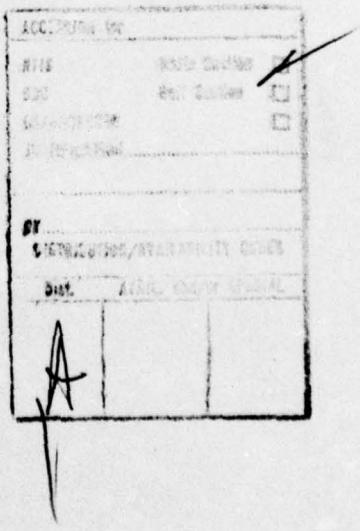

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13. ABSTRACT

Yields on 5400 and 54LS integrated circuits continue to improve as predicted. The exception is on a few lots ~~were~~ where equipment problems or errors resulted in unsatisfactory results.

Designs and design changes are reviewed on all of the integrated circuits.

Yields on the discrete devices are still discouraging. However, the basic designs are good; only processing variations are of concern. It is believed that yields will improve as additional lots are processed during the confirmatory phase.

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FIFTH QUARTERLY PROGRESS REPORT

MANUFACTURING METHODS AND TECHNOLOGY PROGRAM FOR BEAM LEAD SEALED JUNCTION SEMICONDUCTOR DEVICES

The object of this study is to refine the processes required to fabricate beam-lead sealed junction devices in production quantities by manufacturing methods.

Contract No. DAAB07-75-C-0033

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ABSTRACT

Yields on 5400 and 54LS integrated circuits continue to improve as predicted. The exception is on a few lots were equipment problems or errors resulted in unsatisfactory results.

Designs and design changes are reviewed on all of the integrated circuits.

Yields on the discrete devices are still discouraging. However, the basic designs are good; only processing variations are of concern. It is believed that yields will improve as additional lots are processed during the confirmatory phase.

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1.0 INTRODUCTION

The purpose of this manufacturing methods and technology contract is to improve the processing and thus the yields on 35 integrated circuit and discrete devices. The yield goals are 5 percent for the RA108 (60-Gate Array), 10 percent for the integrated circuits and 20 percent for the discretes.

As outlined in Section 2.0, problems in fine-tuning the processes for the required 14 discrete devices provide the greatest challenge to successfully achieving the overall yield goals on the program. As discussed in previous reports, each discrete device is unique in its processing requirements. Each device must be targeted (from a processing standpoint) for selection from what would normally be a family of devices. For example, the 1N5314 is only one of some thirty regulators, and falls at the very end of the distribution curve. Any variation in times, temperatures or other processing variables on any of the discrete devices, means that the specific device will yield low, whereas some other device in the same family might yield quite high. Furthermore, this occurs on the same wafer, i.e. many device types from the family yield on every good wafer.

In comparison, the IC processing is more forgiving; variations in diffusion times and temperatures are not as critical since most of the electrical parameters have broader ranges than the discretes.

This report reviews the progress made during the Fifth Quarter of the program. During this time, 27 engineering samples have been delivered.

Problems have been encountered in laying out the 54LS196 and 54LS197 which have resulted in a schedule slippage on these two devices. This problem will be resolved sometime during the next quarter.

The complete list of devices required on this program is shown in Table I.

TABLE I

NM&T BEAM LEAD DEVICE LIST

DEVICE	FUNCTION	DEVICE	FUNCTION
1N746	3.3V Z	5405	HEX INV O.C.
1N748	3.9V Z	5410	TRIP 3 NAND
1N5314	5.14 ma CURRENT SOURCE REG.	5440	DUAL 4 NAND
2N2484	NPN HIGH GAIN (100)	5473	DUAL JK
2N2907	PNP SWITCH AND AMPLIFIER	54LS04	HEX INV
2N3251	PNP HIGH SPEED SWITCH (200 ns)	54LS08	QUAD 2 AND
2N3467	PNP 1 AMP CORE DRIVER	54LS21	DUAL 4 AND
2N3501	NPN HIGH VOLTAGE (150V)	54LS32	QUAD 2 OR
2N3635	PNP HIGH VOLTAGE (140V)	54LS73	DUAL JK
2N3639	PNP HIGH SPEED SWITCH (20 ns)	54LS74	DUAL D
2N3725	NPN 1 AMP CORE DRIVER	54LS86	QUAD 2 EX OR
2N3960	NPN RF	54LS138	DECODE-DEMUX
2N4260	PNP RF	54LS193	UP-DOWN COUNTER
2N5115	P CHAN JFET	54LS194	4 BIT S.R.
RA108	60 GATE ARRAY	54LS196	DECADE COUNTER
5400	QUAD 2 NAND	54LS197	BINARY COUNTER
5401	QUAD 2 NAND O.C.	54LS253	DUAL 4-1 MUX
5404	HEX INV		

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2.0 DISCRETE DEVICE STATUS

All MM&T discretes are in the confirmatory phase, but some problems are being experienced in transferring the technology from development to production. This was expected, and with the additional engineering support being provided, the problems will be resolved quickly.

The following provides an updated status of all of the discrete devices:

1N746 & 1N748

Several techniques are now being used to provide better quality devices and better targetability. One of the most interesting of these is the addition of a 3-micron-thick intrinsic epitaxial layer on the surface of the starting wafers. This procedure permits elimination of one photo step and diffusion.

The purpose of this diffusion was to provide a low reverse leakage characteristic for the diode. This technique, however, depends on good quality silicon wafers. For low voltage zeners (2.0-5.0 volts) the best silicon available is not of sufficient quality due to the low resistitivies required. The intrinsic cap is independent of this problem; therefore, it is a more viable approach for the low voltage zener. This intrinsic layer also has the feature of providing nearly bulk breakdown voltages which permits the use of higher resistivity starting material to achieve the same voltage. The result of this is to provide a more reliable device, as well as an easier one to manufacture.

One other change is the addition of a phosphorus getter cycle to reduce leakages still further. This process is a part of the standard zener diode procedure at Motorola. It serves the function of providing a "sink" for metallic impurities which are unavoidably diffused into the wafer during processing. This process also serves to "getter" light metal impurities, such as sodium, and provide the devices with better long-term reliability.

In summary, the benefits of this epitaxial layer are as follows:

1. Zener diodes can be manufactured down to 2.4 volts with good yield.
2. The magnitude of the leakage on present devices can be reduced.
3. The process is simpler and less sensitive to defects.
4. The finished device is more reliable due to reduced junction gradient.

Figure 1 shows a cross-sectional comparison of the zener structures described above.

1N5314

The highest probe yield to date was 1 percent. This device is one of 32 current regulators normally processed as a family. Material and process technologies have not been developed to date that will allow specific device processing such as this to a predictable yield.

2N2484

The highest probe yield to date was 5.8 percent. The low current beta requirement demands that surface recombination lifetimes are kept low. Phosphorus gettering is being increased to reduce the effects of heavy metals. Surface states are also affected by thermal stress and a stress-free process is being developed to minimize this.

2N2907A

The highest probe yield to date was approximately 73 percent without the high current parameters being measured. High current measurements were not possible in the past because generated heat could not be removed fast enough. The testing procedure has since been changed to provide the capability of making high current measurements.

2N3251

The highest probe yield to date was 1.7 percent. Adjustments to the base and emitter home-in should improve the final probe yields, and improved techniques for lifetime control should improve the marginal storage time problem.

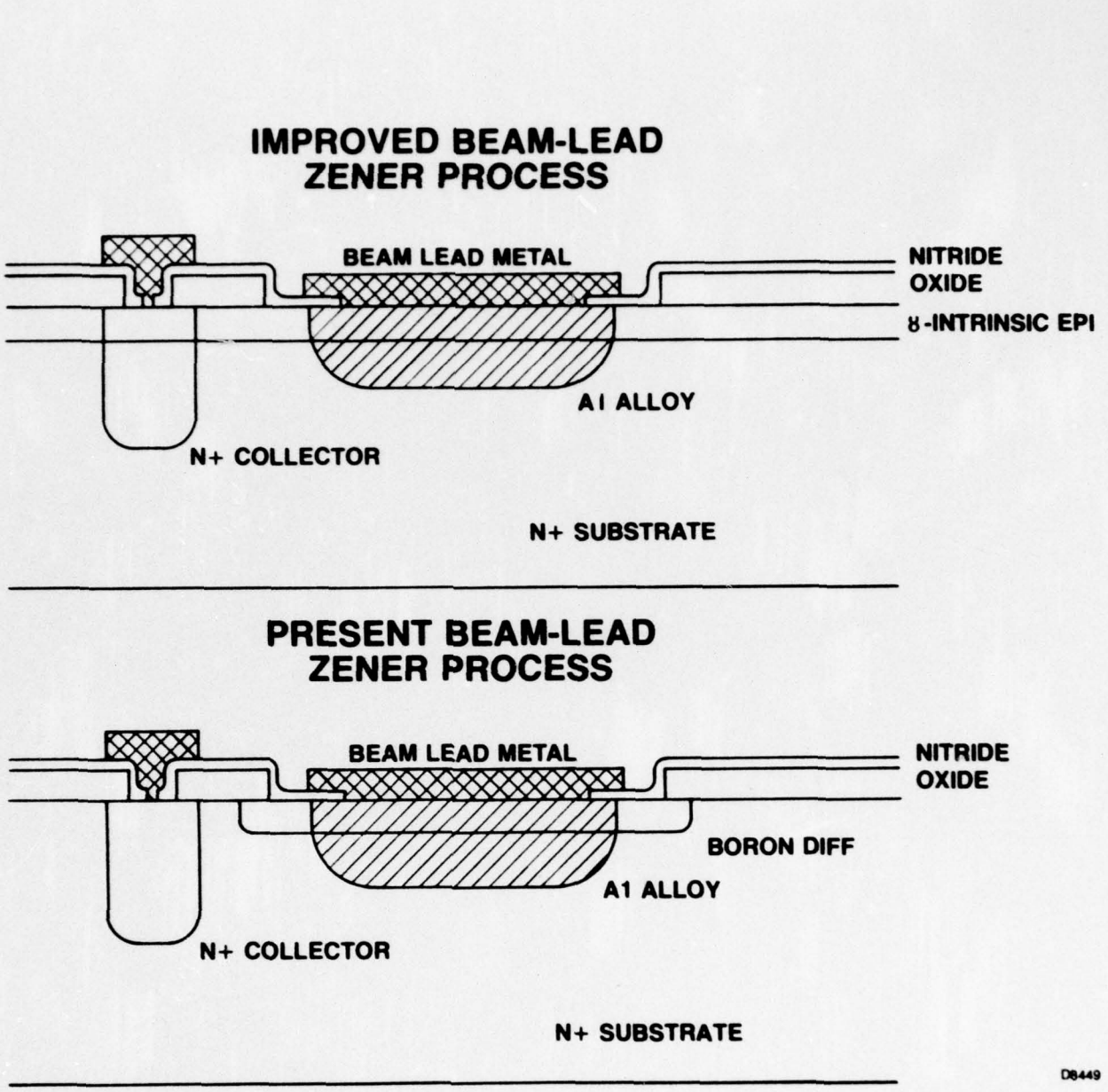

Figure 1. COMPARISON OF ZENER DIODE PROCESSES

2N-3467

The highest probe yield to date was 1.7 percent. The technique to control minority carrier lifetime has been refined and losses incurred in the past should be reduced.

2N-3501

The highest yield to date was 15.9 percent. Rapid scan techniques are being employed to assure epitaxial layer thickness and each wafer is being checked for resistivity. Material changes may be required to reduce the beta kink problems.

2N-3635

The highest probe yield to date was 4.7 percent. Rapid scan evaluation and tighter resistivity controls will all tighten material distribution.

2N-3639

The highest probe yield to date was 52.6 percent. The storage time, as measured on this product is marginal. Therefore, it is imperative that the specific procedure used to control minority carrier lifetime be adjusted to improve the storage time parameters.

2N-3725

The highest probe yield to date was 2 percent. The high gain requirements along with high BV_{CEO} requirements have created some emitter home-in problems. It should also be mentioned that the material that has been processed previously resulted in many good 2N-3724 devices, which are part of the 2N-3725 family.

2N-3960

The highest probe yield to date was 22 percent. The process is being fine-tuned to reflect higher yields.

2N-4260

The highest probe yield to date was 4.2 percent. The process has been modified to increase the P^+ dopant in the collector contact region. This will lower the R_{sat} term, the major reject parameter.

2N-5115

Major photomasking techniques have been developed and the process guidelines are being refined to define the home-in techniques required on this device. No operational devices have been manufactured as yet.

3.0 INTEGRATED CIRCUIT STATUS

3.1 IC PROCESSING

Significant progress has been made during this past quarter with the completion and shipment of 22 samples. These include two first engineering samples, eight second samples, and twelve third samples. In addition, six confirmatory samples have been completed.

Probe yields continue to be more than adequate to meet the contract minimums. (It is estimated that with a probe yield of 26-30 percent, the overall yield requirement of 10 percent can be achieved.) Indeed, the six confirmatory lots have an average probe yield of 57.8 percent. See Figure 2, which is a plot of probe yields during this past quarter.

A slight downward trend during the first half of the time period was largely attributed to high transistor beta readings. This was the result of a minor diffusion furnace modification that was made late in May, 1976. The diffusion cycles have since been adjusted to obtain the proper beta readings.

A malfunction of the platinum sputtering equipment caused low yields on the 5473 (Lot 2). Lots 5400, lot 2, 5401, lot 2 and 5410, lot 2 were probed with test programs that were later discovered to be slightly in error. When these lots are reprobed with the corrected program, it is believed that the yields will be significantly higher.

An operator error with 54LS86, Lot 1, caused a 0 yield on that lot. The wafers apparently were placed in a high temperature furnace at the thick gold plating operation with photoresist on the wafers. The underlying titanium became unetchable with the normal chemical etchants. Many attempts were made to salvage the wafers. Finally, the titanium layer was etched in the fluorine plasma etcher. This indeed removed the titanium, but it also damaged the silicon nitride surface and the gold metallization, causing all die to be visual rejects.

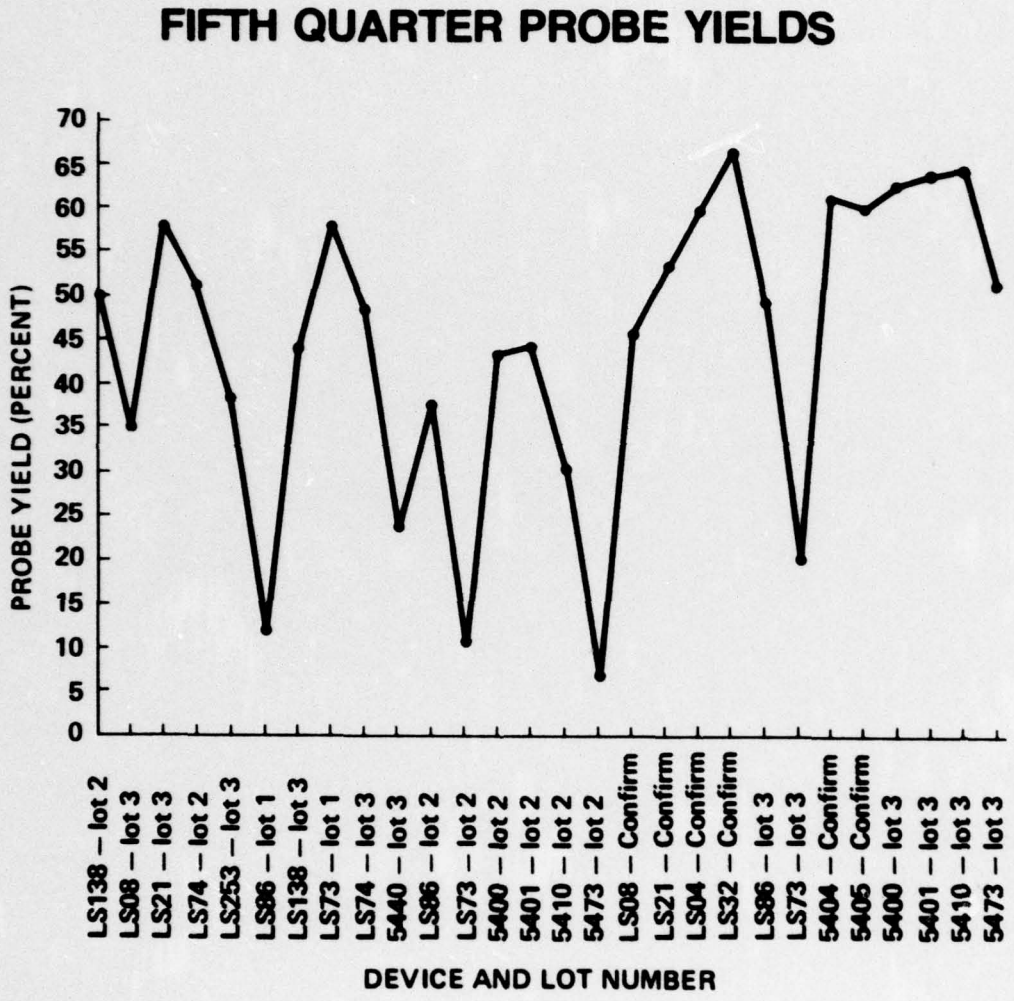

Figure 2. Probe Yield During Fifth Quarter

In spite of all of these problems, one wafer was probed to verify that the mask set was correct. This one wafer yielded 130 good die for a yield of 11.9 percent. But, as stated above, all were rejected for visual reasons.

Figure 3 is a plot of predicated probe yield as a function of die size. The actual probe yields that were obtained since May, 1976, are shown as "X points. Note that approximately half of the lots have yielded within 10 percent of their predicted yield.

Table II shows the results of those circuits that have completed confirmatory processing and have been probed. Note that all of these probe yields are more than adequate for contract requirements.

At present, the 5400, 5401, 5410, 5473, LS74, LS86 and LS138 confirmatory lots are in process.

The mask sets on these seven circuits have been evaluated and corrected. Three circuits are presently receiving mask changes to improve the DC and AC performance over the full specified temperature range. These are the 5440, LS73 and LS253. The design corrections on two of the circuits, the LS253 and the 5440 are completed and masks are being generated.

Starting material on the 60 gate array, the RA108 circuit, should arrive in the first week of October. On two other circuits, the LS193 and LS194, material is presently being processed for the first and second samples. The LS196 and LS197 circuits are still in the mask layout stage.

A summary of the integrated circuit progress to date is given in Table III. Note that almost all circuit types that have been probed have had yields in excess of 45 percent for the best lot. Also, the total number of probed good die DC tested has more than doubled during the past quarter.

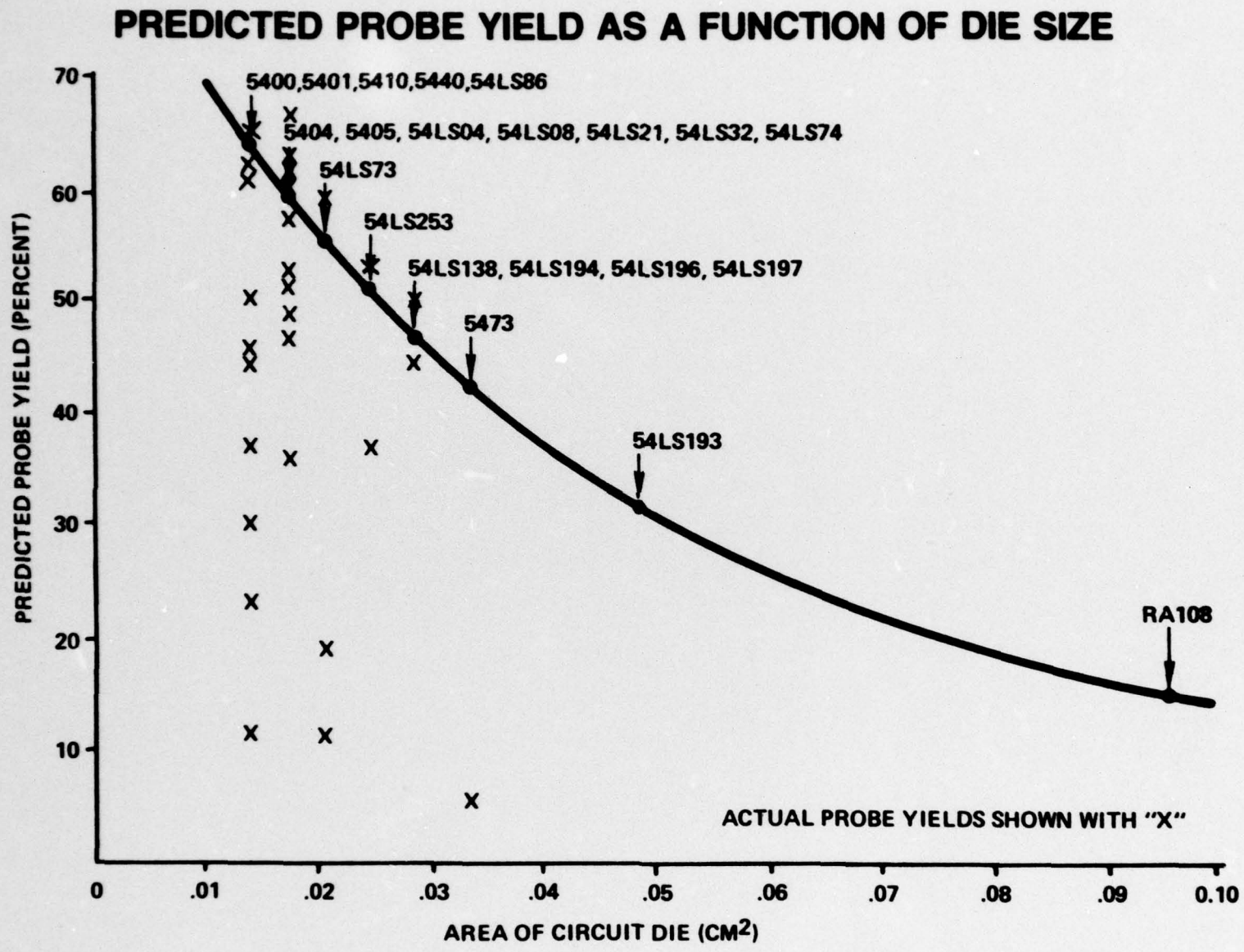

Figure 3. PREDICTED PROBE YIELD AS A FUNCTION OF DIE SIZE

TABLE II

CONFIRMATORY LOTS PROBED DURING AUGUST, 1976

DATE PROBED	DEVICE NUMBER	CIRCUIT PROBE YIELD %	NO. OF GOOD DIE
Aug. 26, 1976	54LS08	46.0	1592
Aug. 26, 1976	54LS21	52.8	1196
Aug. 26, 1976	54LS04	60.1	4,346
Aug. 27, 1976	54LS32	66.5	3992
Aug. 30, 1976	5404	61.3	2401
Augs. 30,1976	5405	59.9	2396

TABLE III

IC PROBE SUMMARY TO DATE

DEVICE	BEST LOT PROBE YIELD %	NUMBER OF LOTS PROCESSED	NUMBER OF PROBED GOOD DIE - DC TESTED
5400	62.4	3	5533
5401	63.6	3	4365
5404	61.3	6	6433
5405	59.9	6	3363
5410	64.2	3	3966
5440	47.3	3	2567
5473	51.6	3	1998
54LS04	69.2	6	8213
54LS08	46.0	4	2701
54LS21	57.6	4	2030
54LS32	66.5	5	11,149
54LS73	58.1	3	4281
54LS74	51.6	3	6433
54LS86	49.1	3	5070
54LS138	49.7	3	1854
54LS193			
54LS194			
54LS196			
54LS197			
54LS253	38.8	3	3921
RA108	-	1	
TOTAL		62	73,877
TOTALS - 3 MONTHS AGO - 6/7/76		41	30,978

3.2 DESIGN

3.2.1 Overview

In general, when a new circuit family concept is realized, a certain amount of trimming and tweaking to optimize performance is required.

Motorola's approach to the 5400 and 54LS circuit families was to provide the industry with a state-of-the-art beam lead logic, i.e. master mask, seal junction technology, as well as one with somewhat improved electrical performance. The concept in doing this was that ECOM would realize greater value added from the contract,and that Motorola would be left with a superior family of devices.

Although problems have been encountered, it is believed that the approach was correct.

Motorola is using a gate structure which improves upon standard 54LS noise margin and threshold at temperature. Although electrical performance of this gate is superior to standard 54LS gates, the silicon real-estate required for implementation is greater. This has presented layout problems since it requires the layout of more complex circuitry (requiring more silicon area) into a pre-determined chip size with fixed beam outs. This has been a rather formidable task. Most of the circuit types layed out to date have required one or more changes. These are listed below:

1. 5400, 5401, 5404, 5405 and 5410

   The input PN diodes were changed to increase input threshold. The output devices were also increased in size to decrease the VOL (output voltage) over temperature. Crossunders in series with the output devices were removed. Removing these output crossunders prevented forward biasing and turning on of a Darlington transistor pair which would lead to excessive current drain at high temperatures.

   These changes were common to all of the above devices and were implemented on them all since test data indicated these changes were necessary.

2. 5440 and 5473

These circuits also required an increase in the size of the output devices to reduce the VCE(s) and lower the output VOL. This problem was encountered due to the fact that the output devices were initially sized correctly for gold doped processing. As Motorola made the decision to implement Schottky technology for this family of devices, this size proved inadequate, due to the higher offset voltage of the Schottky devices. The Schottky devices are faster than conventional gold doped devices because no minority carrier injection ever occurs at the collector-base junction, therefore, no stored charge can ever accumulate in the collector region and slow down turn-off time. Excess base drive is shunted away from injection and flows externally through the Schottky diode. As a consequence, however, since no injection occurs at the collector-base junction, the alpha inverse-becomes vanishingly small and the offset voltage increases logarithmically.

$$V(\text{offset}) \simeq \frac{KT}{q} \ln \frac{1}{\alpha_i}$$

This offset voltage term is added to the VCE(s) and degrades the output voltage minimum. This can only be compensated by creating a larger output device with a lower IR drop in the collector region.

$$* \quad VCE(s) = V(\text{offset}) + I_C (R_1+R_2+R_3)$$

3. Further analysis will detail changes implemented in the 54LS family of circuits.

* See Appendix A, Second Quarterly Report for detailed analysis.

3a. 54LS04 and 54LS05

A problem common to the majority of the 54LS family of circuits (as was the conversion to Schottky technology) was believed to be an inadequate input threshold to insure noise immunity over the full temperature range. Motorola has gone to considerable effort to increase the input threshold level to 0.8 volt at room temperature to insure that the input threshold would still be greater than 0.7 volts at high temperatures. This noise immunity has been achieved at the price of additional space requirements per gate, plus a need to increase gate speed to compensate for each gate triggering higher (and later) on the input waveform. The 54LS input gate structure shown in Figure 4, may be compared with other approaches.

4. 54LS08, 54LS21 and 54LS32

These circuits all require the input gate threshold changes detailed above. In addition, some minor beam-out changes were implemented to the metals mask. These changes were made to generate a consistent family of circuits with common pinouts and allow for future common-carrier/common-substrate implementations.

5. 54LS86

The primary problem with the initial lots was speed. Functionally it was correct; most performance (DC) was acceptable. To increase circuit throughput speed, a Schottky diode in the input structure was changed to a PN type diode. In the off-going mode the stored charge in the PN diode's diffusion capacitance acted to remove base charge from the gate transistor to be switched. This increased speed with no additional sacrifice in power. Additionally, two PN type clamping diodes on the input lines were removed, so that their additional capacitance would not excessively load the circuit. These corrections appear to have been successful.

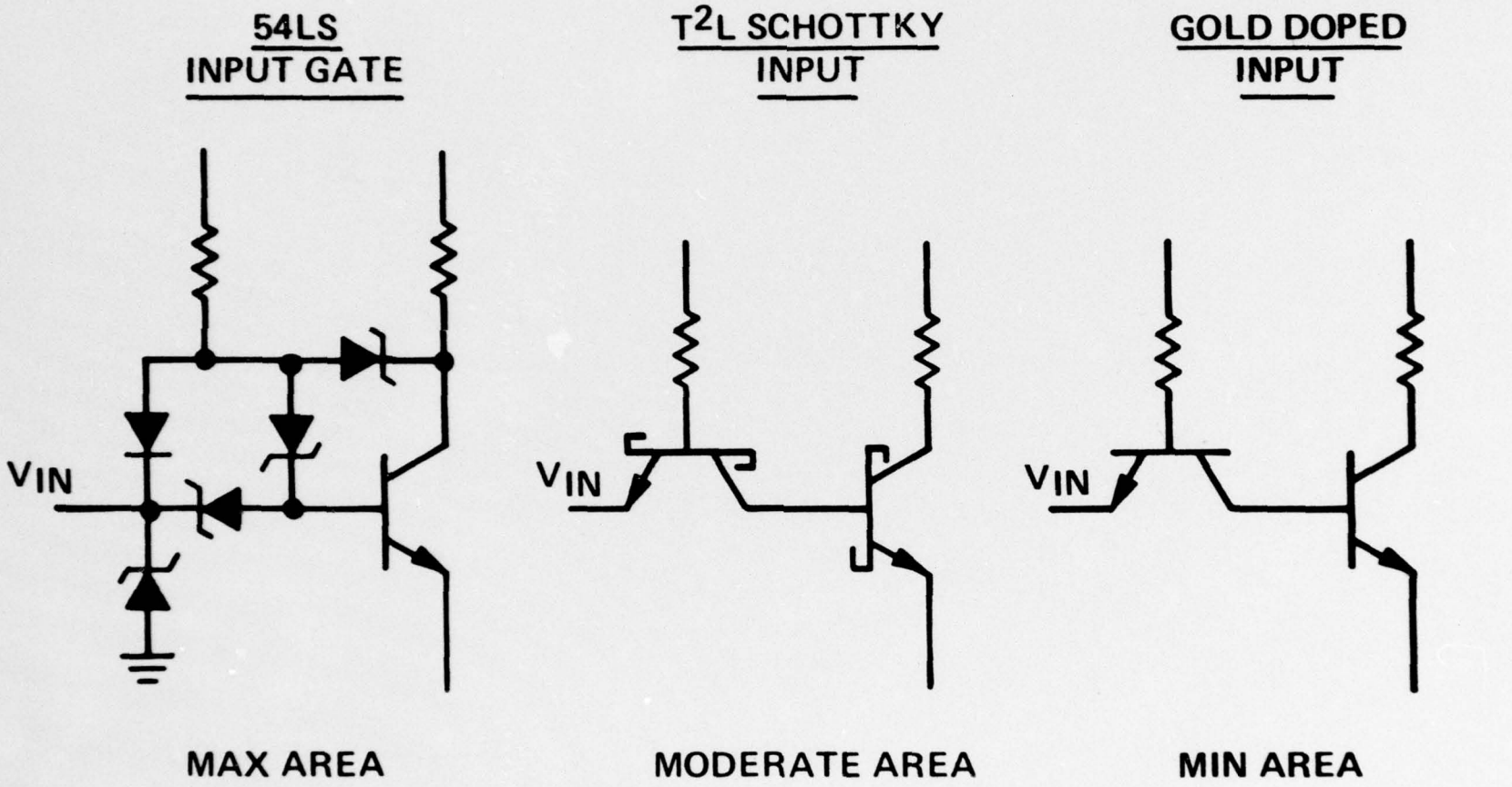

Figure 4. Input Gate Comparison

6. 54LS73

This circuit exhibited a speed problem associated with the maximum toggle frequency, although the propagation speeds were in spec. (See Table IV). This problem was particularly serious, and quite difficult to fix since it was controlled by an internal race condition between different logic elements. Considerable analysis was performed to determine if the circuit could be used adequately in its present configuration, or if a different logic realization would have to be employed. This would require a complete redesign and relayout.

Several engineering changes to the circuit have been proposed to optimize performance as listed below. These are being implemented at present. Whether or not these corrections will be sufficient to increase the nominal toggle frequency will not be confirmed until first samples are available.

54LS73 Proposed Design Changes

1. Change 8K resistors to 6K (4 places)
2. Remove negative transient transistors from clock line (4 places)
3. Change Schottky diodes to PN diodes on Q & $\overline{Q}$ output to master (4 places)
4. Same as above on clock inputs
5. Change 25K resistors to 17K (4 places)
6. Change 12K resistors to 10K (4 places)
7. Change 17K resistors to 12K (4 places)

7. 54LS138

This circuit also had the input gate diode conversion implemented as explained previously. The Schottky diodes were changed to PN diodes to increase the switching speed. In addition to these corrections, some pull-up resistors were increased in value to decrease the power consumption. One of the internal gates was also completely redesigned to achieve a lower device count.

TABLE IV

SPEED PERFORMANCE CHARACTERISTICS
FOR 54LS73

Parameter	Spec.	Typical	Actual
Toggle	30 MHZ	45 MHZ	20 MHZ
TLH	20 Ns	11 Ns	17 Ns
THL	30 Ns	15 Ns	24 Ns

8. 54LS253

The speed-up resistors were changed from 8K to 5.5K to increase the switching speed with more current. One node was particularly slow due to excessive capacitance. Four separate transistors were incorporated into one tub to reduce the overall parasitic capacitance and thus speed-up that node. In addition, several of the internal gate output devices were enlarged to improve the driving capability.

9. 54LS196/7

This circuit has now been layed out three times. More correctly the circuit is in layout for the third time. It is so large, and so complex that it has required considerable changes in design and/or layout in order to fit into the predetermined chip size. The circuit layout is now 90 percent complete.

10. RA108 Metal

The first seven RA108 masks have been completed and material is in process. The RA108 metal is being generated through a computer discretionary software program which is able to realize additional options as well.

4.0 CONCLUSIONS AND PLANS FOR NEXT QUARTER

4.1 CONCLUSIONS

When normally implementing the design, fabrication, testing, redesign, etc. of a new product, it is customary to process a number of lots in order to determine both that the design is sound and that the process will yield satisfactorily. This is particularly true of a process which had not previously been established in production.

In the case of the LS devices, some 30 lots of various device types were manufactured in establishing that process. As pointed out previously, only three lots of each of the discretes (each being unique) were processed in attempting to realize a good process for each type.

It became evident sometime ago that additional sample lots might be required, but it was mutually agree that Motorola would be authorized to proceed with the confirmatory sample processing. If some devices satisfied the contractual requirements, they would be submitted to the Qualification Test Program. In cases where lots failed due to processing variations or errors, new confirmatory samples would be started. This was a wise decision, for the 1N746 failed whereas the 1N748 yielded well. The 1N746 was restarted.

There will be other lots such as these, but future changes in processing the discretes for the most part will be minor. It is believed that all of the confirmatory and pilot production devices will be shipped on schedule.

4.2 PLANS FOR NEXT QUARTER

Additional homing-in techniques will be employed to improve the discrete yields. By the end of the quarter, barring any mishaps in processing, nearly 60 percent of the IC confirmatory devices will have been processed. Some of these are new designs, so a sample of each will be packaged for full AC/DC temperature testing before submitting the balance of the lots to qual tests.